REMARKS

Claims 1-23 and 47-51 are pending in the present application. Claims 1-23 have been amended. Claims 47-51 have been presented herewith. Claims 24-46 have been canceled. Applicant respectfully reserves the right to file a divisional application including canceled claims 24-46.

Priority Under 35 U.S.C. 119

Applicant notes the Examiner's acknowledgment of the Claim for Priority under 35 U.S.C. 119, and receipt of the certified copy of the priority document.

Drawings

Applicant notes the Examiner's acceptance of the drawings as filed along with the present application on April 28, 2006.

Claim Rejections-35 U.S.C. 102

Claims 1-7, 10-15 and 17-22 have been rejected under 35 U.S.C. 102(e) as being anticipated by the Tanida et al. reference (U.S. Patent Application Publication No. 2006/0038300). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The stacked semiconductor device of claim 1 consists of a first semiconductor device, and a second semiconductor device connected with and secured on the first

semiconductor device, whereby the first semiconductor device includes in combination among other features a first multilayer wiring part "on said first circuit elements and configured of a first wiring electrically connected with said first circuit elements and a first insulating material layer, the first wiring and the first insulating material layer being stacked alternately with the first insulating material layer being an uppermost layer"; a first insulating layer "for covering said first insulating material layer of said first multilayer wiring part and provided all over said first semiconductor substrate, said first insulating layer is a support member of said first semiconductor substrate"; and a plurality of first post electrodes "on said first wiring of said first multilayer wiring part and each having a top surface and side surfaces, the top surfaces of said first post electrodes exposed from a surface of said first insulating layer and all the side surfaces of said first post electrodes covered by said first insulating layer". Applicant respectfully submits that the Tanida et al. reference as relied upon by the Examiner does not disclose these features.

The first insulating layer of claim 1 as noted above is a support member of the first semiconductor substrate, and supports the first semiconductor substrate during thinning of the first semiconductor substrate, and also makes handling of the substrate easier. Although not necessarily limited thereto, these features of the first insulating layer may be considered as described in paragraphs [0032], [0069] and [0070] of the present application.

The Examiner has interpreted bump (projection electrode) 12 in Fig. 4 of the Tanida et al. reference as a post electrode of claim 1. However, all the side surfaces of bump 12 in Fig. 4 of the Tanida et al. reference are not covered by a support member of semiconductor substrate 2, as would be necessary to meet the features of claim 1. That is, a first insulating layer is not shown in Fig. 4 of the Tanida et al. reference as a support member covering all sides of bump 12 and as separately provided on a first insulating material layer of a first multilayer wiring part. The Tanida et al. reference thus fails to meet all the features of claim 1.

With further regard to this rejection, the Examiner has interpreted penetration electrode 45 in Fig. 4 of the Tanida et al. reference as the first through-type electrode of claim 1, and rear-side connection surface 45a of penetration electrode 45 as the outside electrode terminal of claim 1. However, the outside electrode terminals of claim 1 are featured specifically as connected to the first through-type electrodes, and thus are not merely a surface of the first through-type electrodes. Although not necessarily limited thereto, this may be appreciated in view of Fig. 1 of the present application. Clearly, rear-side connection surface 45a in Fig. 4 of the Tanida et al. reference is merely a surface of penetration electrode 45, not a separately featured outside electrode terminal connected to penetration electrode 45. The Tanida et al. reference thus fails to meet these further features of claim 1.

Accordingly, Applicant respectfully submits that the stacked semiconductor device of claim 1 distinguishes over the Tanida et al. reference as relied upon by the

Examiner, and that this rejection, insofar as it may pertain to claims 1-7 and 10-15, is improper for at least these reasons.

The semiconductor device of claim 17 includes in combination among other features a multilayer wiring part "on said circuit elements and configured of a wiring electrically connected with said circuit elements and an insulating layer, the wiring and the insulating layer being stacked alternately with the insulating layer being an uppermost layer"; a first insulating layer "for covering said insulating layer of said multilayer wiring part and provided all over said semiconductor substrate, said first insulating layer is a support member of said semiconductor substrate"; and a plurality of post electrodes "on said wiring of said multilayer wiring part and each having a top surface and side surfaces, the top surfaces exposed from a surface of said first insulating layer and all the side surfaces covered by said first insulating layer".

As asserted previously, bump 12 in Fig. 4 of the Tanida et al. reference does not have all side surfaces thereof covered by a support member, as would be necessary to meet the features of claim 17. That is, the Tanida et al. reference does not include the first insulating layer of claim 17. The Tanida et al. reference as relied upon thus fails to meet all the features of claim 17. Applicant therefore respectfully submits that the semiconductor device of claim 17 distinguishes over the Tanida et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 17-22, is improper for at least these reasons.

Claim Rejections-35 U.S.C. 103

Claims 4, 16 and 23 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Tanida et al. reference. Applicant respectfully submits that the Tanida et al. reference as herein relied upon does not overcome the above noted deficiencies as described above with respect to claims 1 and 17, and that this rejection is therefore improper for at least these reasons.

Claims 8 and 9 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Tanida et al. reference in view of the Murata reference (U.S. Patent Application Publication No. 2002/0030266). Applicant respectfully submits that the Murata reference as secondarily relied upon does not overcome the above noted deficiencies of the primarily relied upon prior art, and that this rejection is therefore improper for at least these reasons.

Claims 47-51

The semiconductor device of claim 47 includes in combination among other features a first insulating layer "on an uppermost layer of said multilayer wiring part"; and a first electrode "over the first main surface, the first electrode having top and side surfaces electrically connected with a part of the wiring pattern, the top surface being exposed from a surface of said first insulating layer and all the side surfaces being covered with said first insulating layer".

As asserted previously, bump 12 in Fig. 4 of the Tanida et al. reference does not have all sides thereof covered with a first insulating layer. Applicant therefore respectfully submits that claims 47-51 distinguish over and would not have been obvious in view of the prior art as relied upon by the Examiner for at least these reasons.

Conclusion

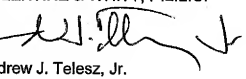
The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE & WHITT, P.L.L.C.



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